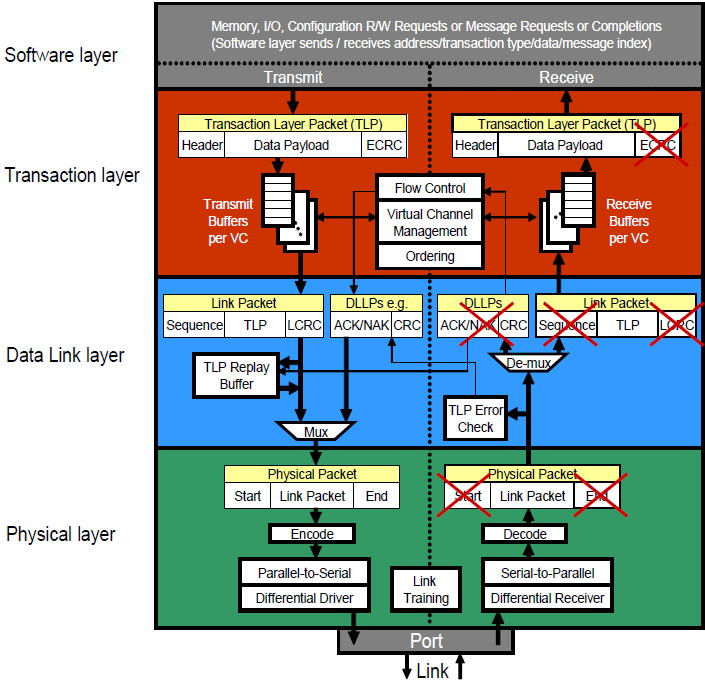


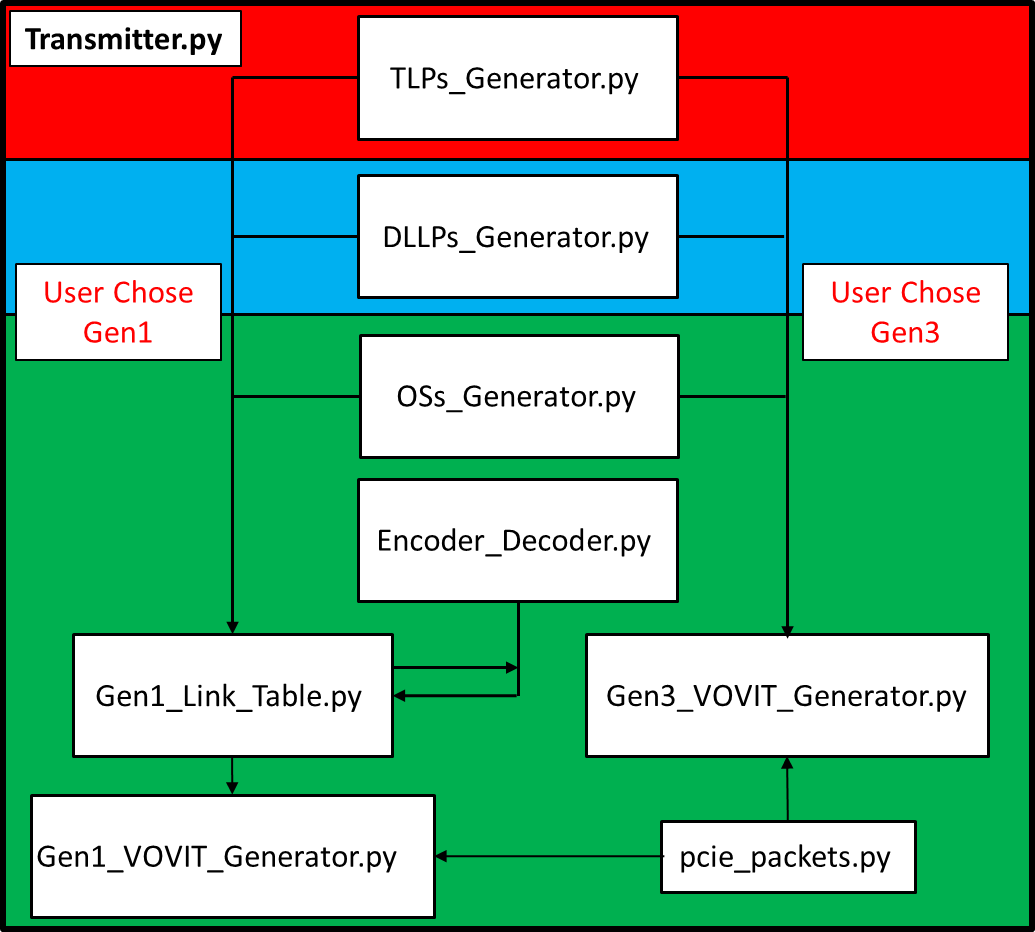
**VOVIT Gen1/3 Traffic Trace**

# **1. Overview**

This Simulator is implemented according to transmitter main logic in the PCIe interconnect fabric.



The main script Transmitter.py acts as transmitter while rest of the scripts invoked according to their parts in the three layers: Transaction, Data Link and Physical.



1. TLPs/DLLPs/OSs\_Generator.py generate random packets.

2. TLP and DLLP packets are identical in both gen1 and gen3. OSs are different.

3. Gen1: We use 8b/10b packets encoding. We can’t encode all packets and then transmit

them all together because of running disparity calculations.

Gen3: We use 128b/130b packets encoding

4. User can choose PCIe generation (1/3).

Gen1: Choose whether or not to perform encoding, create Gen1\_Packets\_List.txt file,

Print Link Symbols Table to shell (Gen1\_Link\_Table.txt will be created).

Gen1\_VOVIT\_Trace.txt will be created.

Gen3: Packets will be encoded, Gen3\_Packets\_List.txt, Gen3\_Link\_Table.txt and

Gen3\_VOVIT\_Trace.txt files will be created.

5. Gen3 packets and VOVIT Trace Generation logic remained the same. The original

vovit\_generator.py integrated into Transmitter.py in order to support both gen 1 and

gen 3.

6. This simulator requires python 3 with prettytable and colorama packages installed.

For more information, refer here:

<https://pypi.org/project/colorama/>

<https://pypi.org/project/prettytable/>

# **2. Main Script - Transmitter.py**

1. The script gets user's arguments using the Argparse module (a command-line parsing

module in the python standard library. For more information, refer here:

<https://docs.python.org/3/library/argparse.html#module-argparse> )

2. Arguments list:

2.1. –gX , X=1/3 , required=True , PCIe Gen 1 or 3 Packets.

2.2. –tN , N=Number , required=False , Generated TLPs count.

2.3. –dN , N=Number , required=False , Generated DLLPs count.

2.4. –oN , N=Number , required=False , Generated OSs count.

\* at least one count has to be bigger than zero.

2.5. –e , required=False , Encode gen1 packets

2.6. –l , required=False , Print gen1 link symbols table

2.7. –c , required=False , Color printed gen1 link symbols table

\* use 2.8 when printing table to shell. The Gen1\_Link\_Table.txt file will be ruined

because of the colors characters.

Important: VOVIT packets are generated from Link Table symbols. Currently, if you are using the -e option (10bit encoded symbols) it will affect the VOVIT packets correctness. this can be changed if required.

3. User Chose Gen1:

3.1. Transmitter.py will add Sequence number and LCRC to TLPs in the Data Link Layer.

3.2. Transmitter.py will handle TLPs and DLLPs Framing in the Physical Layer

3.3. Gen1\_Link\_Table.py will “transmit the packets” = create and draw the link

symbols table.

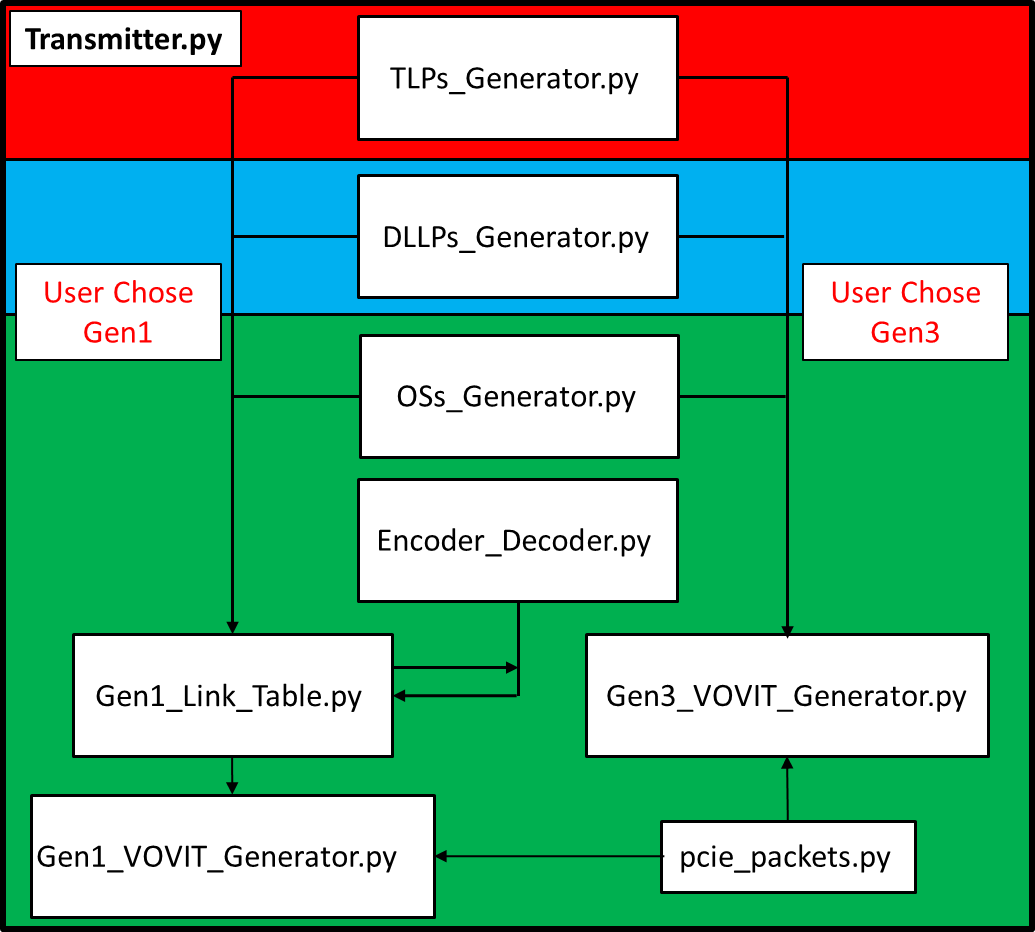
3.4. If requested, Gen1\_Link\_Table.py will use Encoder\_Decoder.py to encode each

packet before transmission according to the 8b/10b encoding scheme.

3.5. Gen1\_VOVIT\_Generator.py generates the Gen1\_VOVIT\_Trace.txt from the new

link symbols table.

3.6. pcie\_packets.py contains TLP, DLLP, OS classes being used by

 Gen1/Gen3\_VOVIT\_Generator.py

4. User Chose Gen3:

Gen3\_VOVIT\_Generator.py gets TLPs/DLLPs/Oss

and handles the rest:

- Creates the link symbol table:

Gen3\_Link\_Table.txt according to

128b/130b encoding scheme.

- Creates VOVIT Trace: Gen3\_VOVIT\_Trace.txt

- Creates Gen3\_Packets\_List.txt

* pcie\_packets.py contains TLP,DLLP,OS classes being used by Gen1/Gen3\_VOVIT\_Generator

# **3. Packets Generators**

The TLPs/DLLPs/OSs\_Generator.py scripts generate random packets according to user's input (packets number of each type).

Later on all packets are combined into one packets list and the list gets shuffled to create random packets order.

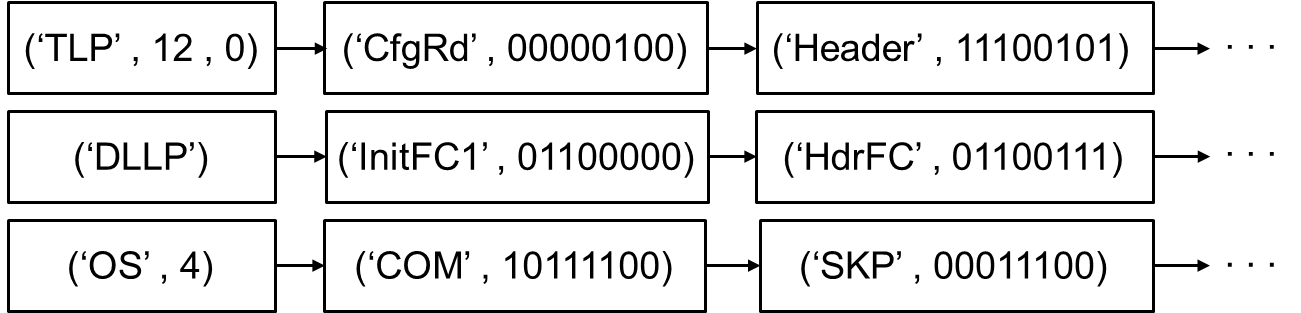
Gen1:

Each Packet represented by a list of tuples. The first tuple contains 'meta data' on that packet for later use. Rest of tuples contain a string and a value representing the suitable symbol.

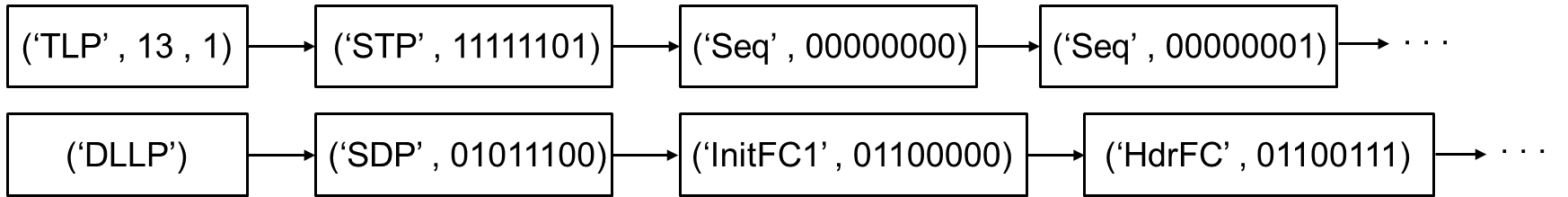
TLP first tuple: ( 'TLP' , Header length , Data Payload length )

DLLP first tuple: ( 'DLLP' ) , all DLLPs are 8 symbols long

OS first tuple: ( 'OS' , packet length )



Later on the Transmitter.py adds Sequence number (real by order) and LCRC to TLPS and perform framing to DLLPS and TLPS.



* Currently there is no TLP prefix
* Most symbols are random generated
* For more packets information please refer to Appendixes 6.4 – 6.6 in this document.

Gen3:

Each packet is a string in hexadecimal format.

TLP: 040000010401d20f0510011c

DLLP: c004b265

OS: aa000000000000000000000000000000

# **4. Symbols Encoding**

The Encoder\_Decoder.py stores all symbols encoding/decoding values according to the 8bit/10bit scheme.

1. Sections 6.1. through 6.3. describe the two possible 10bit encoding values for each

symbol (Control and Data) in the 8b/10b encoding scheme.

2. Each row contains the following:

2.1. Symbol token, string.

2.2. Symbol 8b value, binary.

2.3. Two possible 10b encoded values, binaries.

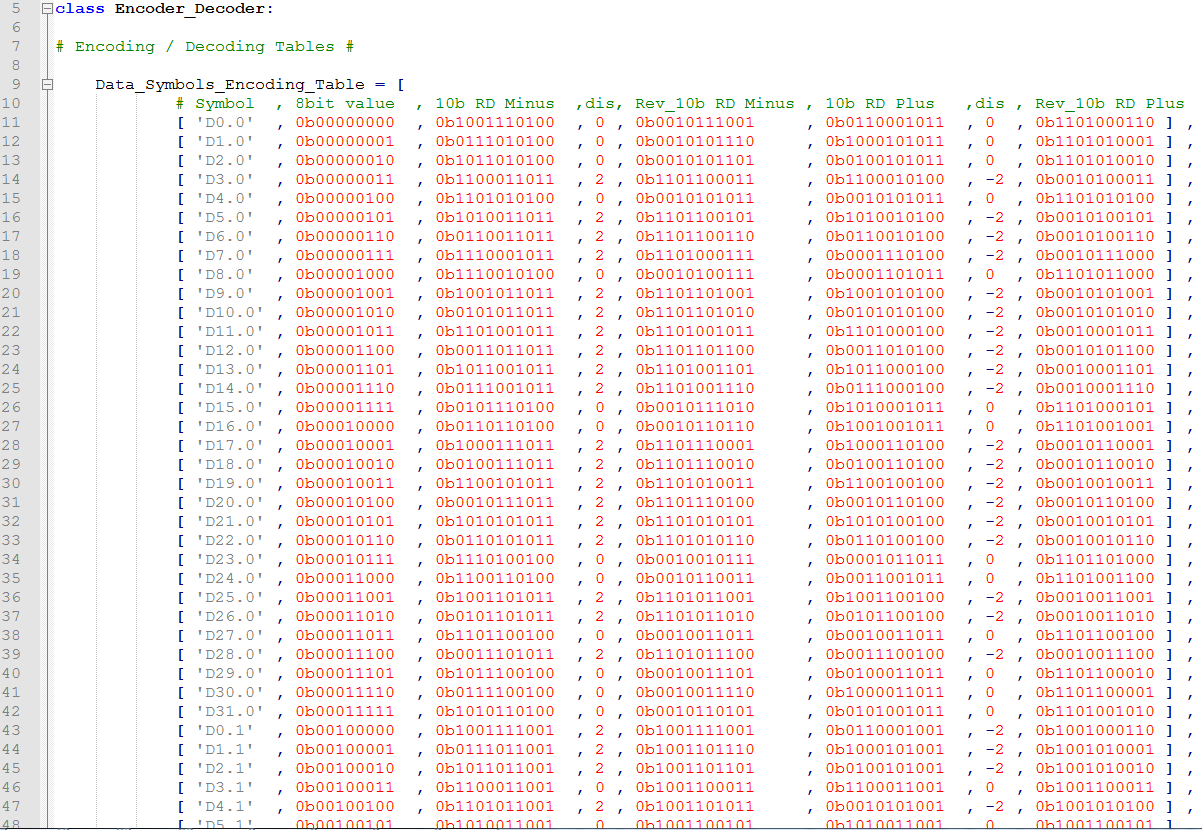
2.4. Disparity of each 10b encoded value for calculating current running disparity,

numbers.

2.5. Reverse binaries of the 10b encoded values because the encoded values are

transmitted in reverse order.

3. Auxiliary scripts for creating the encoding/decoding tables are provided.



* For Gen3 Packets the 128b/130b encoding takes place in Gen3\_VOVIT\_Generator.py and are not discussed in this document.

# **5. Link Symbols Table**

The Gen3\_VOVIT\_Generator.py creates the link symbol table and won't be discussed in this document.

1. The Gen1\_Link\_Table.py gets the shuffled packets list and creates the link symbols table. It follows the following rules of a transmitter in the PCIe interconnect fabric, taken from "PCI Express® Base Specification Revision 5.0 Version 1.0 ":

1.1. Ordered Sets are always transmitted serially on each Lane, such that a full Ordered

Set appears simultaneously on all Lanes of a multi-Lane Link.

1.2. The Framing mechanism uses Special Symbol K28.2 “SDP” to start a DLLP and Special Symbol K27.7 “STP” to start a TLP.

1.3. The Special Symbol K29.7 “END” is used to mark the end of either a TLP or a DLLP.

1.4. The conceptual stream of Symbols must be mapped from its internal representation, which is implementation dependent, onto the external Lanes.

1.5. The Symbols are mapped onto the Lanes such that the first Symbol (representing Character 0) is placed onto Lane 0; the second is placed onto Lane 1; etc.

1.6. The x1 Link represents a degenerate case and the mapping is trivial, with all Symbols placed onto the single Lane in order.

1.7. When no packet information or special Ordered Sets are being transmitted, the Transmitter is in the Logical Idle state. During this time idle data must be transmitted. The idle data must consist of the data byte 0 (00 Hexadecimal), scrambled according to the rules of Section 4.2.1.3 and 8b/10b encoded according to the rules of Section 4.2.1.1, in the same way that TLP and DLLP Data Symbols are scrambled and encoded.

1.8. Likewise, when the Receiver is not receiving any packet information or special Ordered Sets, the Receiver is in Logical Idle and shall receive idle data as described above.

1.9. During transmission of the idle data, the SKP Ordered Set must continue to be transmitted as specified in Section 4.2.7.

1.10. For the following rules, “placed” is defined to mean a requirement on the Transmitter to put the Symbol into the proper Lane of a Link.

1.10.1. TLPs must be framed by placing an STP Symbol at the start of the TLP and an END

Symbol or EDB Symbol at the end of the TLP (see Figure 4-5).

1.10.2. A properly formed TLP contains a minimum of 18 symbols between the STP and END

or EDB Symbols. If a received sequence has less than 18 symbols between the STP

and END or EDB symbols, the receiver is permitted to treat this as a Receiver Error.

◦ If checked, this is a reported error associated with the Receiving Port (see Section

6.2).

1.10.3. DLLPs must be framed by placing an SDP Symbol at the start of the DLLP and an END

Symbol at the end of the DLLP (see Figure 4-6).

1.10.4. Logical Idle is defined to be a period of one or more Symbol Times when no

information: TLPs, DLLPs or any type of Special Symbol is being

Transmitted/Received. Unlike Electrical Idle, during Logical Idle the Idle Symbol

(00h) is being transmitted and received.

◦ When the Transmitter is in Logical Idle, the Logical Idle data (00h) shall be

transmitted on all Lanes. This is scrambled according to the rules in Section 4.2.1.3.

◦ Receivers must ignore incoming Logical Idle data, and must not have any

dependency other than scramble sequencing on any specific data patterns.

1.10.5. For Links wider than x1, the STP Symbol (representing the start of a TLP) must be

placed in Lane 0 when starting Transmission of a TLP from a Logical Idle Link

condition.

1.10.6. For Links wider than x1, the SDP Symbol (representing the start of a DLLP) must be

placed in Lane 0 when starting Transmission of a DLLP from a Logical Idle Link

condition.

1.10.7. The STP Symbol must not be placed on the Link more frequently than once per

Symbol Time.

1.10.8. The SDP Symbol must not be placed on the Link more frequently than once per

Symbol Time.

1.10.9. As long as the above rules are satisfied, TLP and DLLP Transmissions are permitted

to follow each other successively.

1.10.10. One STP Symbol and one SDP Symbol may be placed on the Link in the same

Symbol Time.

1.10.11. Links wider than x4 can have STP and SDP Symbols placed in Lane 4\*N, where N is

a positive integer. For example, for x8, STP and SDP Symbols can be placed in

Lanes 0 and 4; and for x16, STP and SDP Symbols can be placed in Lanes 0, 4, 8, or

12.

1.10.12. For xN Links where N is 8 or more, if an END or EDB Symbol is placed in a Lane K,

where K does not equal N-1, and is not followed by a STP or SDP Symbol in Lane

K+1 (i.e., there is no TLP or DLLP immediately following), then PAD Symbols must

be placed in Lanes K+1 to Lane N-1.

◦ For example, on a x8 Link, if END or EDB is placed in Lane 3, PAD must be placed

in Lanes 4 to 7, when not followed by STP or SDP.

1.10.13. The EDB Symbol is used to mark the end of a nullified TLP. Refer to Section 3.6.2.1

for information on the usage of EDB.

1.10.14. Receivers may optionally check for violations of the rules of this section. These

checks are independently optional (see Section 6.2.3.4). If checked, violations are

Receiver Errors, and are reported errors associated with the Port (see Section 6.2).

2. Before transmitting DLLPs/TLPs (= add packets to link table), the script simulates a logical idle state with random length (including zero) by transmitting random number of IDLE (0x00) symbols.

3. If requested, Encoder\_Decoder.py will be called to encode each symbol before adding it

to the link table.

4. If requested, the link symbols table can be printed to shell and its symbols can be

colorized.

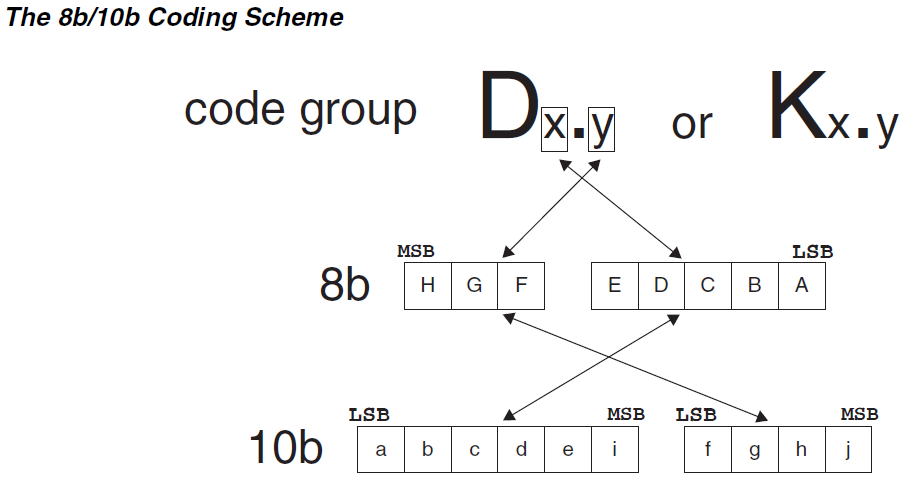
5. If requested, the script will create Gen1\_Packets\_List.txt which lists the generated

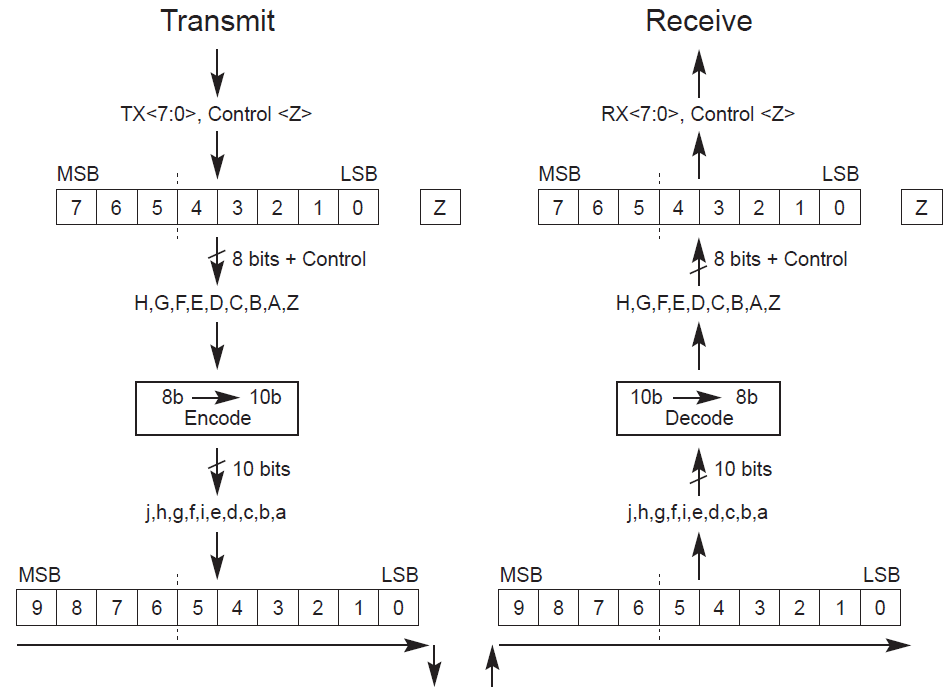
packets.

# **6. Appendixes**

## **6.1. 8b/10b Code Mapping**

The 8b/10b encoder converts 8-bit code groups into 10-bit codes. The code groups include 256 data characters named Dx.y and 12 control characters named Kx.y.

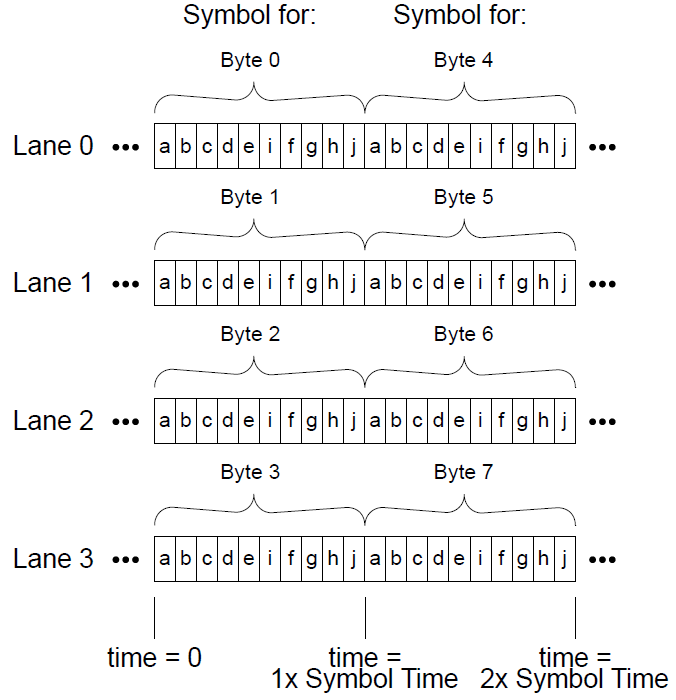




The coding scheme breaks the original 8-bit data into two blocks, 3 most significant bits (y) and 5 least significant bits (x). From the most significant bit to the least significant bit, they are named as H, G, F and E, D, C, B, A. The 3-bit block is encoded into 4 bits named j, h, g, f. The 5-bit block is encoded into 6 bits named

i, e, d, c, b, a. As seen in the above figures, the 4-bit and 6-bit blocks are then combined into a 10-bit encoded value. The control bit in conjunction with the data character is used to identify when to encode one of the 12 control characters (Kx.y).

The bits of a Symbol are placed on a Lane starting with bit “a” and ending with bit “j”.



## **6.2. DC Balance and Disparity**

### **6.2.1. DC Balance and Run Length**

A DC-balanced serial data stream means that it has the same number of 0s and 1s for a given length of data stream. DC-balance is important for certain media as it avoids a charge being built up in the media.

The run-length is defined as the maximum numbers of contiguous 0s or 1s in the serial data stream. A small run length data stream provides data transitions within a small length of data. Data transitions are essential for clock recovery.

### **6.2.2. Disparity**

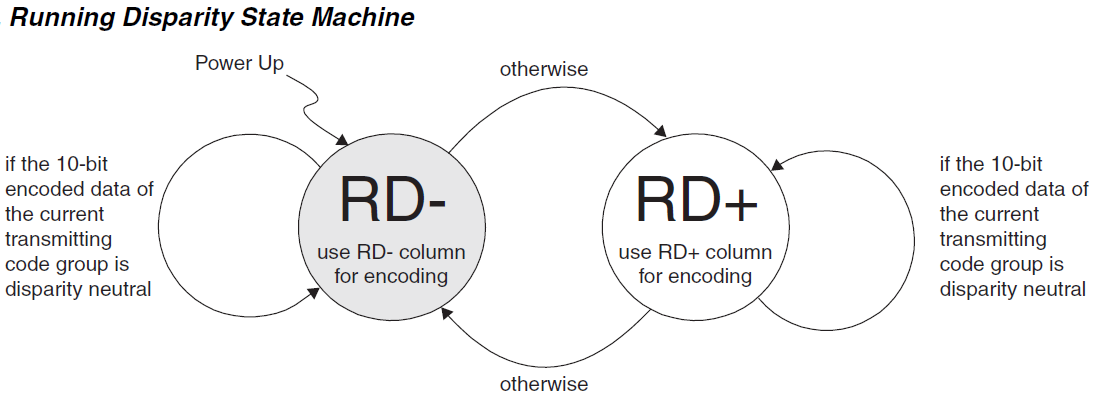
In order to create a DC-balanced data stream, the concept of disparity is employed to balance the number of 0s and 1s. The disparity of a block is calculated by the number of 1s minus the number of 0s. The value of a block that has a zero disparity is called disparity neutral. If both the 4-bit and 6-bit blocks are disparity neutral, a combined 10-bit encoded data will be disparity neutral as well. This will create a perfect DC-balanced code. However, this is not possible. Because only 6 out of the 16 possible values of the 4-bit block are disparity neutral, they are not enough for encoding the 8 values of the 3-bit block. Likewise, only 20 values of the 6-bit block are disparity neutral and they are not enough for encoding the 32 values of the 5-bit block. Because both the 4-bit and 6-bit blocks have an even number of bits, the disparity is not possible to be +1 or -1. Therefore, the values with a disparity of +2 and -2 are also used in the 8b/10b coding scheme.

Concatenating the 4-bit and 6-bit blocks together generates the 10-bit encoded value. Note that some of the encoded values have two possible values, one with a disparity value of +2 and the other with a disparity value of -2. The 8b/10b coding scheme was designed to combine the values of the 4-bit and 6-bit blocks perfectly so that the worst case disparity value of the 10-bit code group will be at most +2

or -2. For example, the 4-bit encoded values with disparity value +2 will not be combined with the 6-bit encoded values with disparity value +2 because this will create a 10-bit value with disparity value +4.

### **6.2.3. Running Disparity**

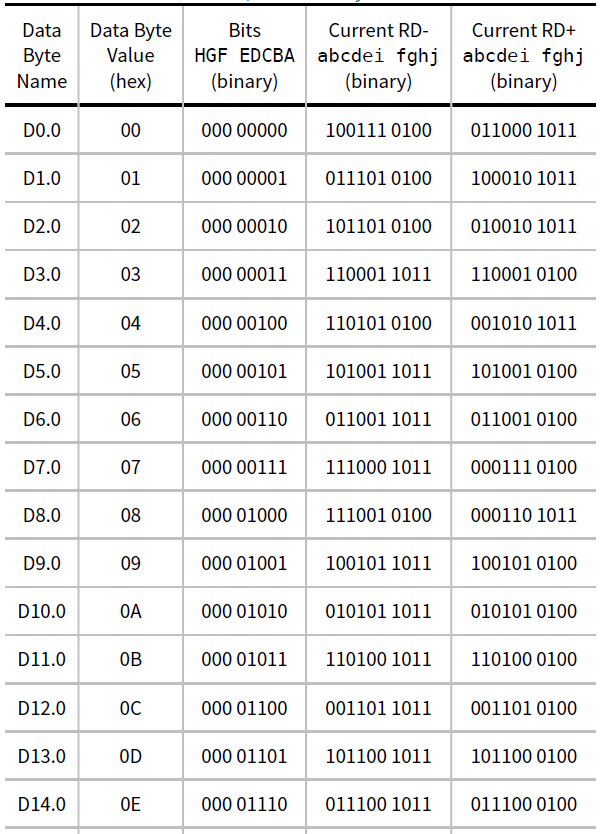
Since the worst disparity of the 10-bit encoded data value is either +2 or -2, it is still possible that more 10-bit encoded data values with +2 (or -2) disparity are transmitted through the serial data stream. In this case, the data stream will no longer be DC-balanced. In order to maintain a DC-balance data stream, each code group will be converted to one of the two possible values referred as RD- and RD+. The RD- disparity will be either +2 or 0 (disparity neutral) and the RD+ disparity will be either -2 or 0. The encoder will pick one of the two values based on the calculation of current Running Disparity. The transmitter assumes a negative Running Disparity (RD-) at start up. When an 8-bit data is encoding, the encoder will use the RD- column for encoding. If the 10-bit data been encoded is disparity neutral, the Running Disparity will not be changed and the RD- column will still be used. Otherwise, the Running Disparity will be changed and the RD+ column will be used instead. Similarly, if the current Running Disparity is positive (RD+) and a disparity neutral 10-bit data is encoded, the Running Disparity will still be RD+. Otherwise, it will be changed from RD+ back to RD- and the RD- column will be used again. The state diagram describes how the current Running Disparity is calculated.



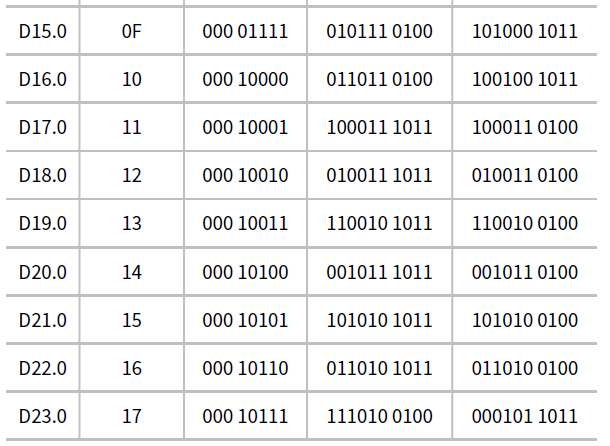
## **6.3. 8b/10b Symbol Codes**

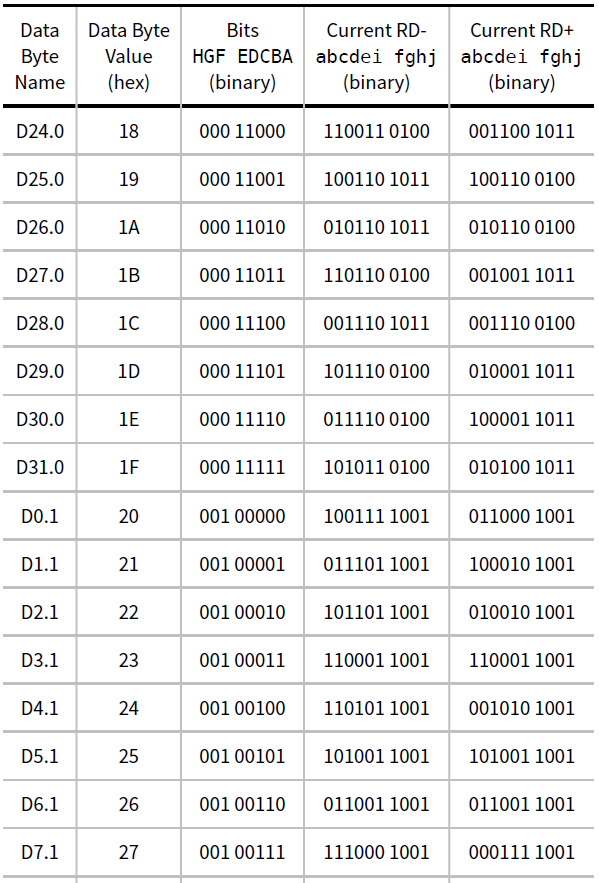
### **6.3.1. 8b/10b Data Symbol Codes**

#### D0.0 – D14.0

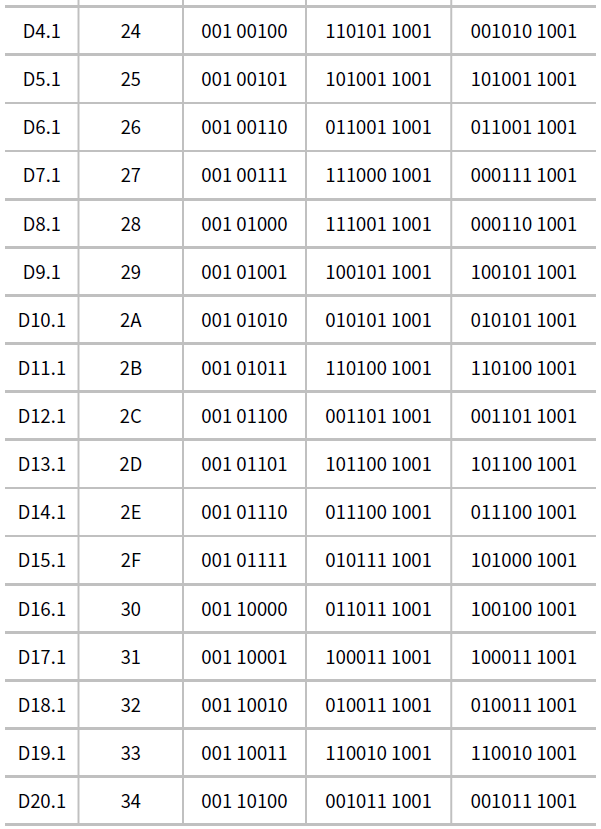


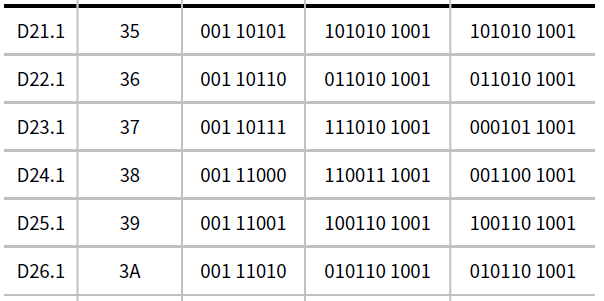
#### D15.0 – D3.1



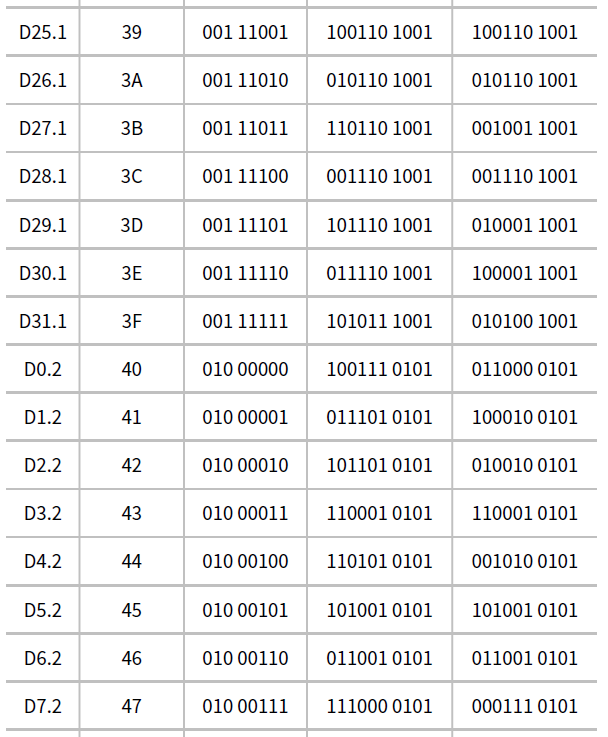


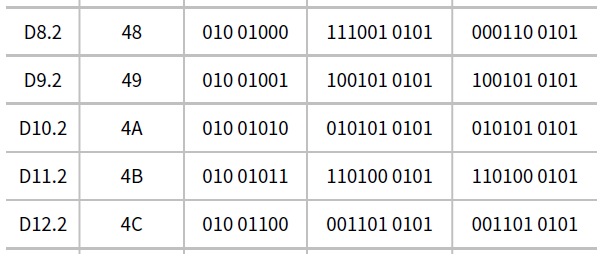
#### D4.1 – D24.1



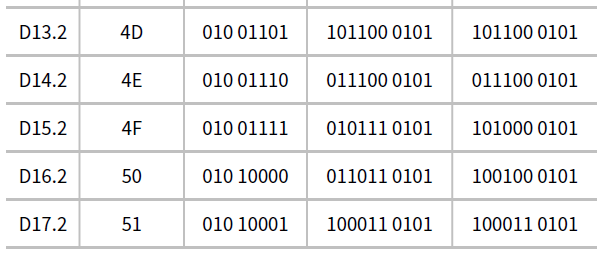


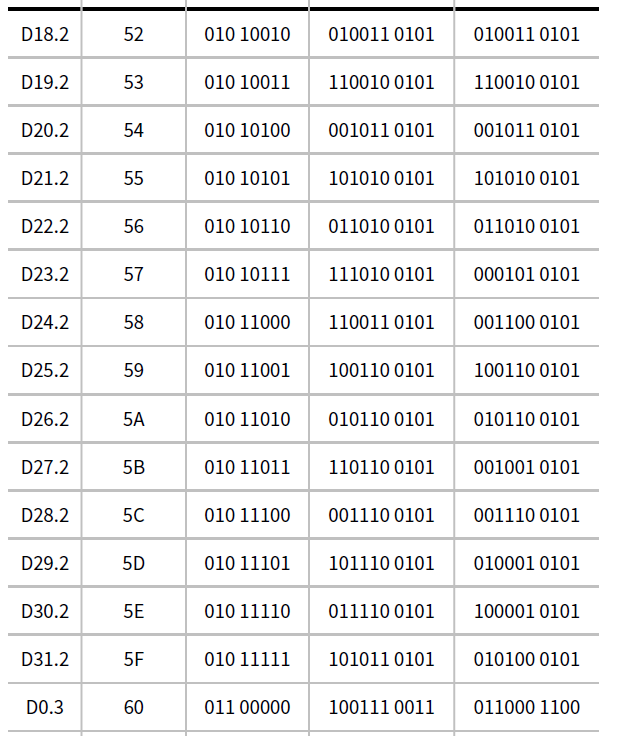
#### D25.1 – D12.2



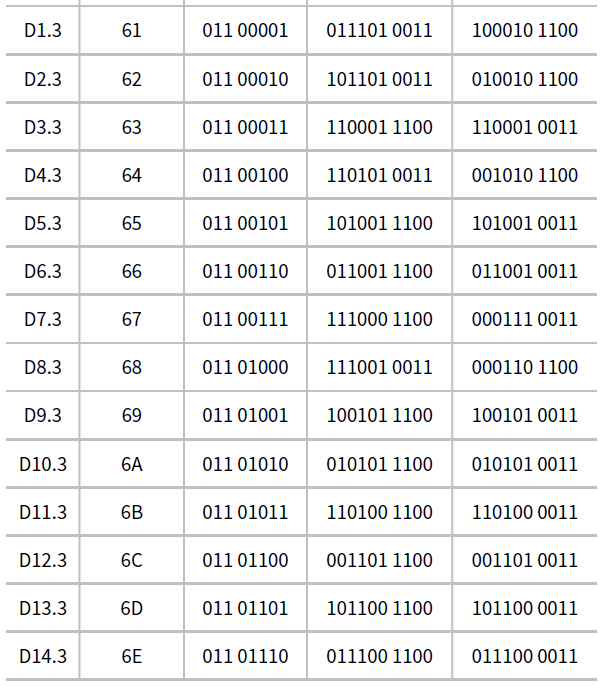


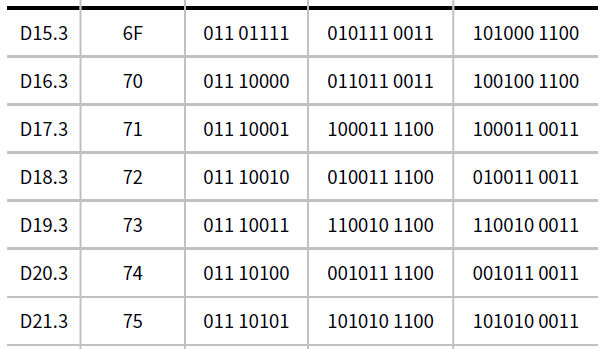
#### D13.2 – D0.3



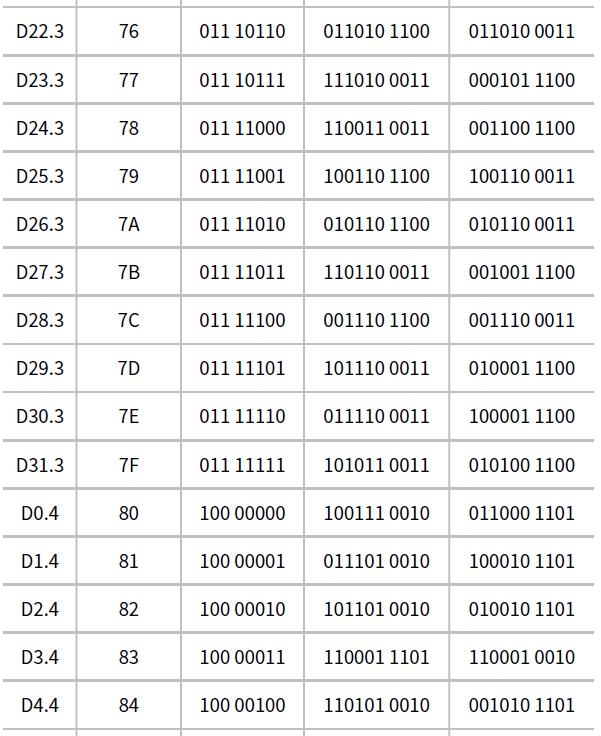


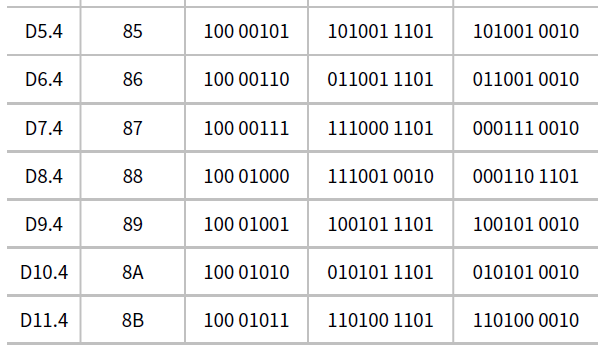
#### D1.3 - D21.3





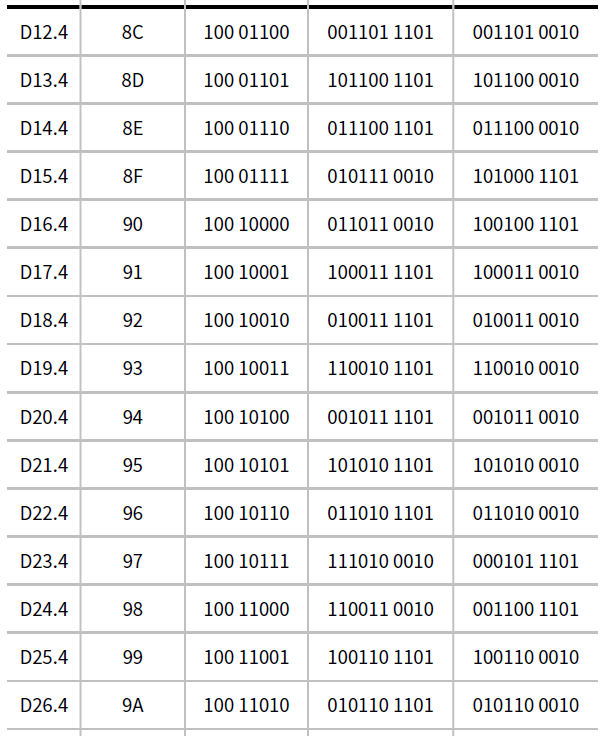
#### D22.3 – D10.4

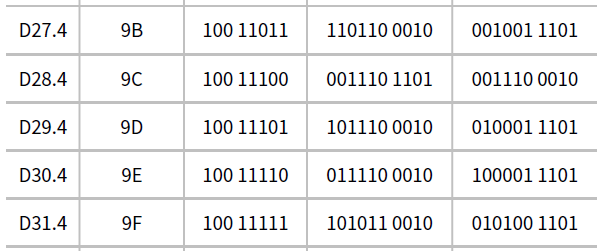




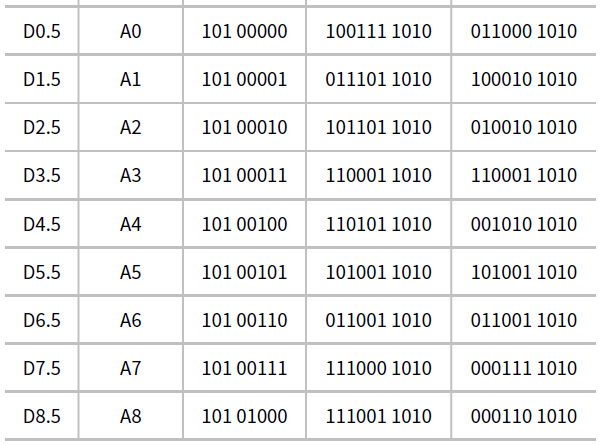
#### D11.4 – D31.4

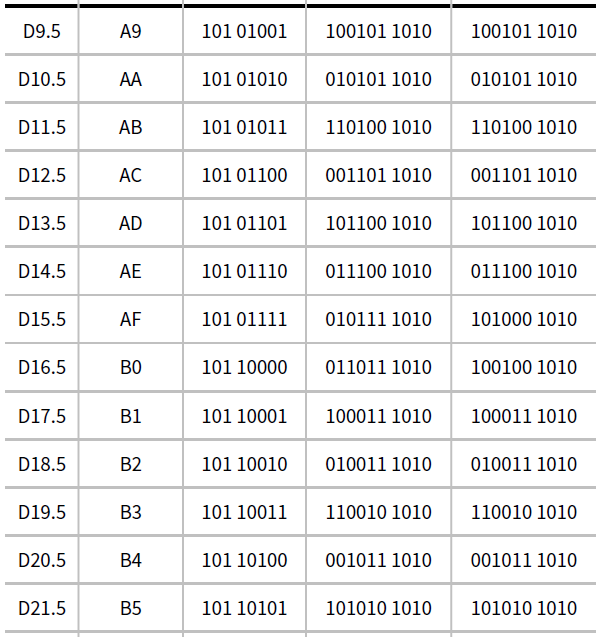




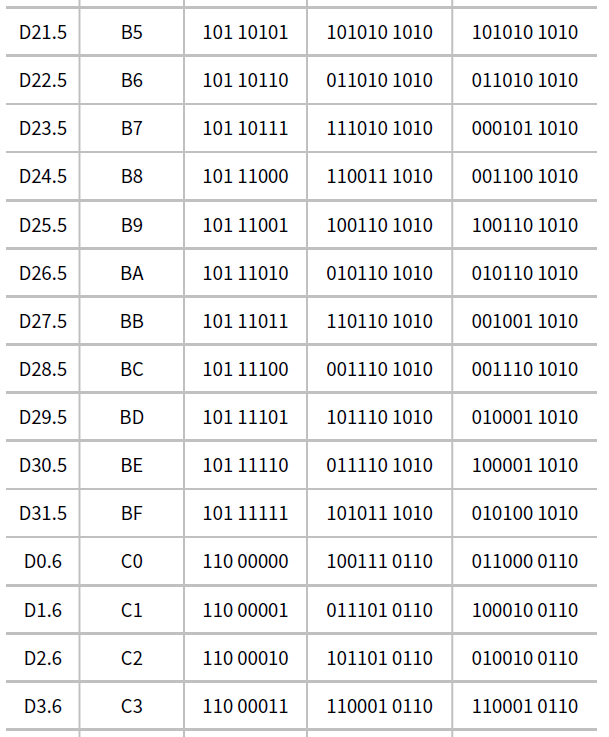


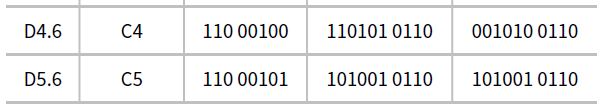
#### D0.5 – D20.5

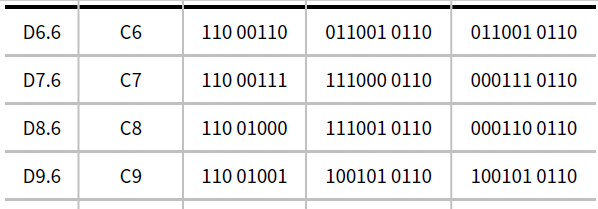




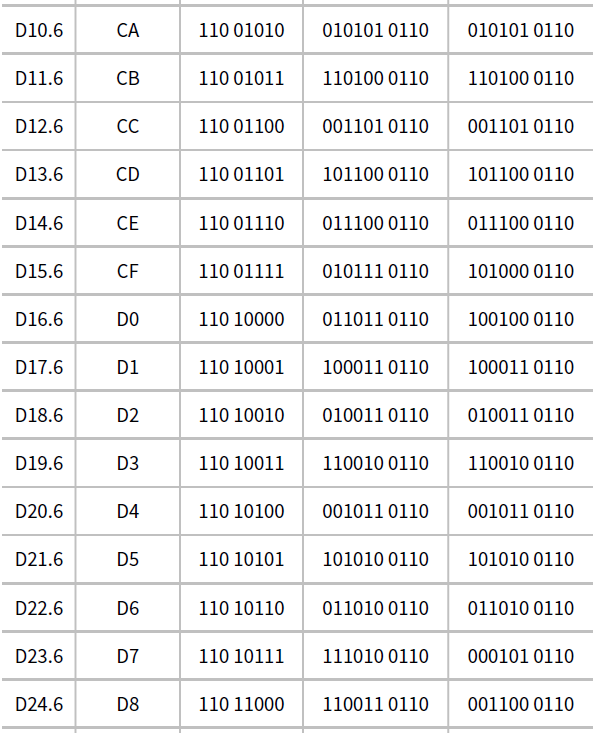
#### D21.5 – D9.6

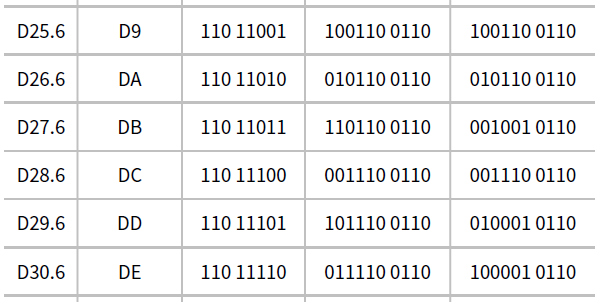




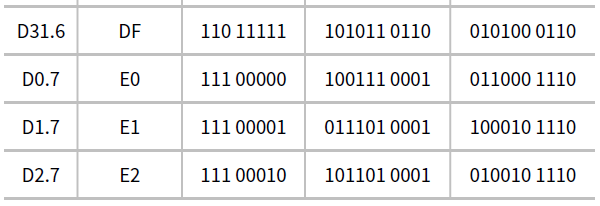


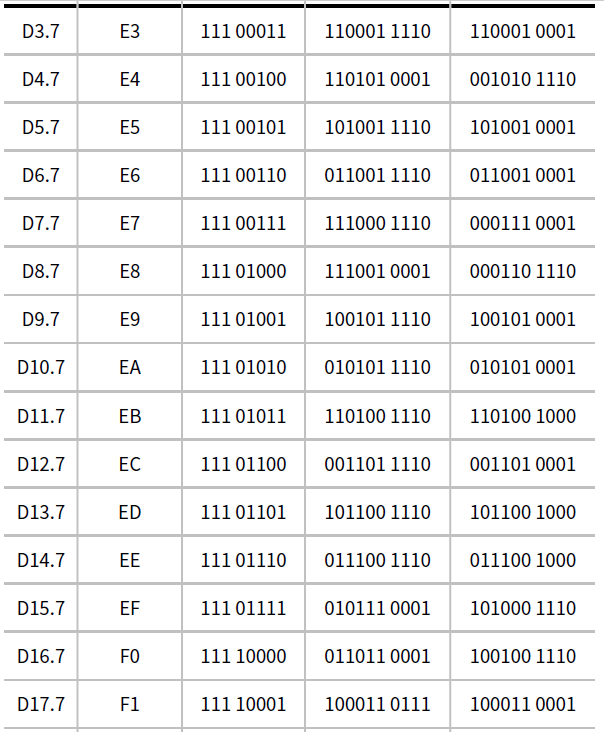
#### D10.6 – D30.6



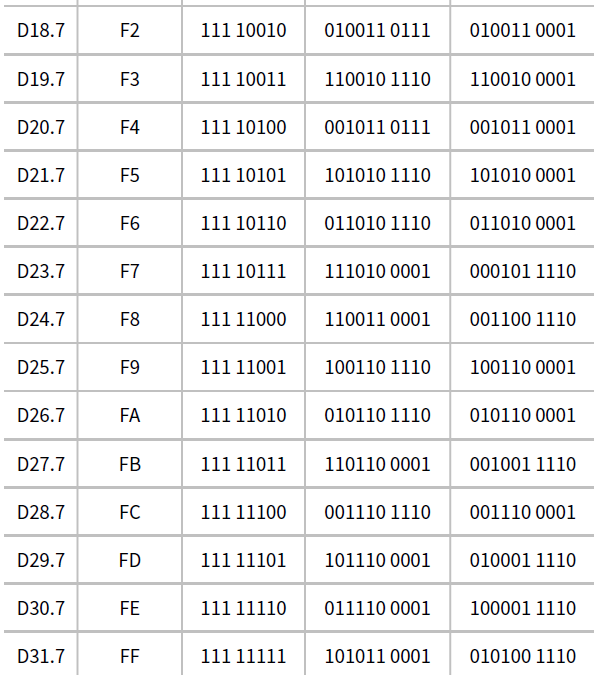


#### D31.6 – D17.7



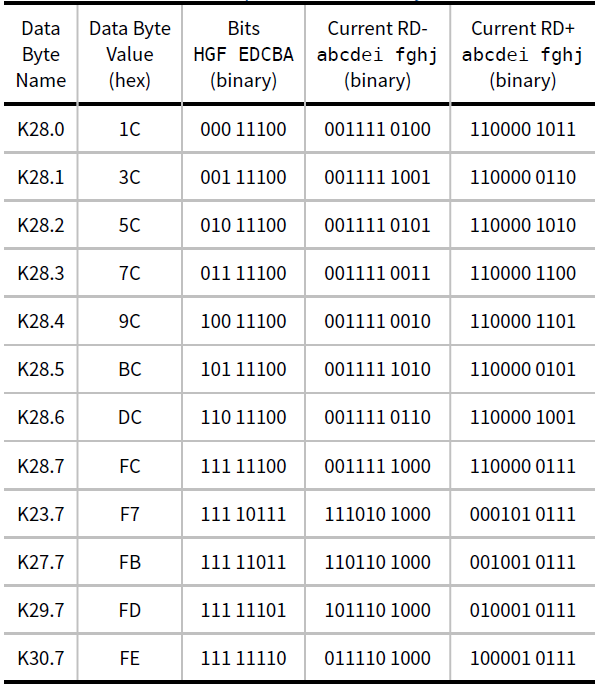


#### D18.7 – D31.7



### **6.3.2. 8b/10b Control Symbol Codes**

#### K28.0 – K30.7



SKP

FTS

SDP

IDL

COM

EIE

PAD

STP

END

EDB

## **6.4. Ordered Sets (Gen 1)**

### **6.4.1. Training Sequences**

Training sequences are composed of Ordered Sets used for initializing bit alignment, Symbol alignment and to exchange physical Layer parameters. Training sequences (TS1 or TS2 or Modified TS1 or Modified TS2) are transmitted consecutively and can only be interrupted by SKP Ordered Sets or, for data rates other than 2.5 GT/s, EIEOS Ordered Sets.

#### 6.4.1.1. TS1 (Training Sequence 1)

|  |  |
| --- | --- |
| Symbol Number | Description |
| 0 | • When operating at 2.5 or 5.0 GT/s: COM (K28.5) for Symbol alignment.  • When operating at 8.0 GT/s or above: Encoded as 1Eh (TS1 Ordered Set). |
| 1 | Link Number.  • Ports that do not support 8.0 GT/s or above: 0-255, PAD.  • Downstream Ports that support 8.0 GT/s or above: 0-31, PAD.  • Upstream Ports that support 8.0 GT/s or above: 0-255, PAD.  • When operating at 2.5 or 5.0 GT/s: PAD is encoded as K23.7.  • When operating at 8.0 GT/s or above: PAD is encoded as F7h. |
| 2 | Lane Number within Link.  • When operating at 2.5 or 5.0 GT/s: 0-31, PAD. PAD is encoded as K23.7.  • When operating at 8.0 GT/s or above: 0-31, PAD. PAD is encoded as F7h. |
| 3 | N\_FTS. The number of Fast Training Sequences required by the Receiver: 0-255. |
| 4 | Data Rate Identifier  BIT 0 - Reserved for future Data Rate.  BIT 1 - 2.5 GT/s Data Rate Supported. Must be set to 1b.  BIT 2 - 5.0 GT/s Data Rate Supported. Must be set to 1b if Bit 3 is 1b.  BIT 3 - 8.0 GT/s Data Rate Supported. Must be set to 1b if Bit 4 is 1b.  BIT 4 - 16.0 GT/s Data Rate Supported. Must be set to 1b if Bit 5 is 1b.  BIT 5 - 32.0 GT/s Data Rate Supported.  ***BIT 6 - Autonomous Change***/***Selectable De-emphasis***.  • Downstream Ports: This bit is defined for use in the following LTSSM states: Polling.Active, Configuration.  Linkwidth.Start, and Loopback.Entry. In all other LTSSM states, it is Reserved.  • Upstream Ports: This bit is defined for use in the following LTSSM states: Polling.Active, Configuration,  Recovery, and Loopback.Entry. In all other LTSSM states, it is Reserved.  BIT 7 - speed\_change. This bit can be set to 1b only in the Recovery.RcvrLock LTSSM state. In all other LTSSM  states, it is Reserved. |
| 5 | Training Control  ***BIT 0 - Hot Reset bit***  0b - Deassert  1b - Assert  ***BIT 1 - Disable Link bit***  0b - Deassert  1b - Assert  ***BIT 2 - Loopback bit***  0b - Deassert  1b- Assert  ***BIT 3 - Disable Scrambling bit*** (2.5 GT/s and 5.0 GT/s data rates)  0b - Deassert  1b - Assert  Reserved (other data rates)  ***BIT 4 - Compliance Receive bit*** (5.0 GT/s and above data rates, optional at 2.5 GT/s)  0b - Deassert  1b – Assert  Ports that support 5.0 GT/s and above data rate(s) must implement the Compliance Receive bit. Ports that support  only 2.5 GT/s data rate may optionally implement the Compliance Receive bit. If not implemented, the bit is Reserved.  ***BIT 5 - Transmit Modified Compliance Pattern in Loopback***. See Section 4.2.6.10.1.  ***BIT 7:6 - Enhanced Link Behavior Control***  ***00b - Full Equalization required***  Modified TS1/TS2 Ordered Sets not supported.  ***01b - Equalization bypass to highest rate support***  Modified TS1/TS2 Ordered Sets not supported.  Indicates intention to perform 32.0 GT/s equalization when set by Loopback Master. See  Section 4.2.3 and Section 4.2.6.10.1.  ***10b - No Equalization needed***  Modified TS1/TS2 Ordered Sets not supported  A device advertising this capability must support Equalization bypass to highest rate. See  Section 4.2.3.  ***11b - Modified TS1/TS2 Ordered Sets supported***  Equalization bypass options specified in Modified TS1/TS2 Ordered Sets.  These bits are defined for use in Polling and Configuration when **LinkUp**=0b and 32.0 GT/s or higher data  rates are supported and in Loopback by the Loopback Master when 32.0 GT/s or higher data rates are  supported. In all other cases, these bits are Reserved. |
| 6 | When operating at 2.5 or 5.0 GT/s:  • Standard TS1 Ordered Sets encode this Symbol as a TS1 Identifier, D10.2 (4Ah).  • EQ TS1 Ordered Sets encode this Symbol as follows:  ◦ For Equalization at 8.0 GT/s Data Rate:  ***BIT 2:0 - Receiver Preset Hint***. See Section 4.2.3.2.  ***BIT 6:3 - Transmitter Preset***. See Section 4.2.3.2.  BIT 7 - Set to 1b.  ◦ For Equalization at 32.0 GT/s or higher Data Rate:  ***BIT 0 - Transmitter Precode Request*** - See Section 4.2.2.5.  BIT 2:1 - Reserved  BIT 6:3 - Transmitter Preset. See Section 4.2.3.2.  BIT 7 - Set to 1b.  When operating at 8.0 GT/s or higher data rate:  BIT 1:0 - Equalization Control (EC). These bits are only used in the Recovery.Equalization and Loopback LTSSM  states. See Section 4.2.6.4.2 and Section 4.2.6.10. In all other LTSSM states, they must be set to 00b.  BIT 2 - Reset EIEOS Interval Count. This bit is defined for use in the Recovery.Equalization LTSSM state. See Section  4.2.6.4.2 and Section 4.2.4.3. In all other LTSSM states, it is Reserved.  BIT 6:3 - Transmitter Preset. See Section 4.2.3 and Section 4.2.6.  BIT 7 - Use Preset/Equalization Redo. This bit is defined for use in the Recovery.Equalization, Recovery.RcvrLock  and Loopback LTSSM states. See Section 4.2.6.4.1, Section 4.2.6.4.2 and Section 4.2.6.10. In all other  LTSSM states, it is Reserved. |
| 7 | When operating at 2.5 or 5.0 GT/s: TS1 Identifier. Encoded as D10.2 (4Ah).  • When operating at 8.0 GT/s or higher:  BIT 5:0 - FS when the EC field of Symbol 6 is 01b (see Section 4.2.3.1). Otherwise, Pre-cursor Coefficient  for the current data rate of operation.  ***BIT 6 - Transmitter Precoding on***. This bit is defined for use in the Recovery state for use at 32.0 GT/s or  higher. See Section 4.2.2.5. In all the other cases, it is Reserved.  **BIT 7 - Retimer Equalization Extend bit**. This bit is defined for use in the Recovery.Equalization  LTSSM state when operating at 16.0 GT/s or higher data rate. In all other LTSSM states and  when operating at 8.0 GT/s, it is Reserved. |
| 8 | When operating at 2.5 or 5.0 GT/s: TS1 Identifier. Encoded as D10.2 (4Ah).  • When operating at 8.0 GT/s or higher data rate:  BIT 5:0: LF when the EC field of Symbol 6 is 01b (see Section 4.2.3.1). Otherwise, Cursor Coefficient for  the current data rate of operation.  BIT 7:6: Reserved. |
| 9 | When operating at 2.5 or 5.0 GT/s: TS1 Identifier. Encoded as D10.2 (4Ah).  • When operating at 8.0 GT/s or higher data rate:  BIT 5:0: Post-cursor Coefficient for the current data rate of operation.  ***BIT 6: Reject Coefficient Values bit***. This bit can only be set to 1b in specific Phases of the Recovery.  Equalization LTSSM State. See Section 4.2.6.4.2. In all other LTSSM states, it must be set to 0b.  BIT 7: Parity (P). This bit is the even parity of all bits of Symbols 6, 7, and 8 and bits 6:0 of Symbol 9. Receivers  must calculate the parity of the received bits and compare it to the received Parity bit.  Received TS1 Ordered Sets are valid only if the calculated and received Parity match. |
| 10 – 13 | • When operating at 2.5 or 5.0 GT/s: TS1 Identifier. Encoded as D10.2 (4Ah).  • When operating at 8.0 GT/s or above: TS1 Identifier. Encoded as 4Ah. |
| 14 – 15 | • When operating at 2.5 or 5.0 GT/s: TS1 Identifier. Encoded as D10.2 (4Ah).  • When operating at 8.0 GT/s or above: TS1 Identifier (encoded as 4Ah) or a DC Balance Symbol. |

#### 6.4.1.2. TS2 (Training Sequence 2)

|  |  |
| --- | --- |
| Symbol Number | Description |
| 0 | • When operating at 2.5 or 5.0 GT/s: COM (K28.5) for Symbol alignment.  • When operating at 8.0 GT/s or above: Encoded as 2Dh (TS2 Ordered Set). |
| 1 | Link Number.  • Ports that do not support 8.0 GT/s or above: 0-255, PAD.  • Downstream Ports that support 8.0 GT/s or above: 0-31, PAD.  • Upstream Ports that support 8.0 GT/s or above: 0-255, PAD.  • When operating at 2.5 or 5.0 GT/s: PAD is encoded as K23.7.  • When operating at 8.0 GT/s or above: PAD is encoded as F7h. |
| 2 | Lane Number within Link.  • When operating at 2.5 or 5.0 GT/s: 0-31, PAD. PAD is encoded as K23.7.  • When operating at 8.0 GT/s or above: 0-31, PAD. PAD is encoded as F7h. |
| 3 | N\_FTS. The number of Fast Training Sequences required by the Receiver: 0-255. |
| 4 | Data Rate Identifier  BIT 0 - Reserved for future Data Rate.  BIT 1 - 2.5 GT/s Data Rate Supported. Must be set to 1b.  BIT 2 - 5.0 GT/s Data Rate Supported. Must be set to 1b if Bit 3 is 1b.  BIT 3 - 8.0 GT/s Data Rate Supported. Must be set to 1b if Bit 4 is 1b.  BIT 4 - 16.0 GT/s Data Rate Supported. Must be set to 1b if Bit 5 is 1b.  BIT 5 - 32.0 GT/s Data Rate Supported.  ***BIT 6 -*** Autonomous Change/Selectable De-emphasis/Link Upconfigure Capability. This bit is defined for use in  the following LTSSM states: Polling.Configuration, Configuration.Complete, and Recovery. In all other  LTSSM states, it is Reserved.  BIT 7 - speed\_change. This bit can be set to 1b only in the Recovery.RcvrLock LTSSM state. In all other LTSSM  states, it is Reserved. |
| 5 | Training Control  ***BIT 0 - Hot Reset bit***  0b - Deassert  1b - Assert  ***BIT 1 - Disable Link bit***  0b - Deassert  1b - Assert  ***BIT 2 - Loopback bit***  0b - Deassert  1b- Assert  ***BIT 3 -*** Disable Scrambling bit in 2.5 GT/s and 5.0 GT/s data rates; Reserved in other data rates  0b - Deassert  1b - Assert  ***BIT 4 - Retimer Present bit*** in 2.5 GT/s data rate. Reserved in other data rates.  0b - No Retimers present  1b – One or more Retimers present  ***BIT 5 - Two Retimers Present bit*** in 2.5 GT/s data rate. Reserved in other data rates. Ports that support 16.0 GT/s  data rate or higher must implement this bit. Ports that support only 8.0 GT/s data rate or lower are permitted  to implement this bit.  0b - Zero or one Retimers present  01 - Two or more Retimers present  ***BIT 7:6 - Enhanced Link Behavior Control***  ***00b - Full Equalization required***  Modified TS1/TS2 Ordered Sets not supported.  ***01b - Equalization bypass to highest rate support***  Modified TS1/TS2 Ordered Sets not supported.  ***10b -*** No Equalization needed,  A device advertising this capability must support Equalization bypass to highest rate. See  **#sect-link-equalization**.  Modified TS1/TS2 Ordered Sets not supported  ***11b*** - Modified TS1/TS2 Ordered Sets supported,  Equalization bypass options specified in Modified TS1/TS2 Ordered Sets.  These bits defined for use in Polling and Configuration when **LinkUp**=0 and 32.0 GT/s or higher data rate  is supported. In all other cases, Bits 7:6 are Reserved. |
| 6 | When operating at 2.5 or 5.0 GT/s:  ◦ Standard TS2 Ordered Sets encode this Symbol as a TS2 Identifier, D5.2 (45h).  ◦ EQ TS2 Ordered Sets encode this Symbol as follows:  ▪ For Equalization at 8.0 GT/s Data Rate:  ***BIT 2:0 - Receiver Preset Hint***.  ***BIT 6:3 - Transmitter Preset***.  BIT 7 - Set to 1b.  ◦ For Equalization at 32.0 GT/s or higher Data Rate:  ***BIT 0 - Transmitter Precode Request*** -  BIT 2:1 - Reserved.  BIT 6:3 - Transmitter Preset.  BIT 7 - Set to 1b.  When operating at 8.0 GT/s or higher data rate:  BIT 3:0 – Reserved  BIT 5:4 - ***Equalization Request Data Rate***.  00b - 8.0 GT/s  10b - 16.0 GT/s  01b - 32.0 GT/s  11b – Reserved  These bits are defined for use in the Recovery.RcvrCfg LTSSM state. In all other LTSSM states, they are Reserved.  See Section 4.2.3 for usage and recognize that these bits are non-sequentially encoded for purposes  of backwards compatibility.  ***BIT 6 - Quiesce Guarantee***. This bit is defined for use in the Recovery.RcvrCfg LTSSM state. In all other  LTSSM states, it is Reserved.  ***BIT 7 - Request Equalization***. This bit is defined for use in the Recovery.RcvrCfg LTSSM state. In all other  LTSSM states, it is Reserved. |
| 7 | When operating at 2.5 or 5.0 GT/s: TS2 Identifier. Encoded as D5.2 (45h).  • When operating at 8.0 GT/s or above:  ◦ Standard TS2 Ordered Sets encode this Symbol as a TS2 Identifier, 45h.  ◦ 128b/130b EQ TS2 Ordered Sets encode this Symbol as follows:  BIT 0 - Transmitter Precode Request for operating at 32.0 GT/s or higher Data Rate. See Section  4.2.2.5. This bit is Reserved if the 128b/130b EQ TS2 is sent for equalization at data rates  of 8.0 GT/s or 16.0 GT/s.  BIT 2:1 - Reserved  BIT 6:3 - 128b/130b Transmitter Preset. See Section 4.2.3.2.  BIT 7 - Set to 1b.  This definition is only valid in the Recovery.RcvrCfg LTSSM state when Preset values are being communicated. |
| 8 - 13 | • When operating at 2.5 or 5.0 GT/s: TS2 Identifier. Encoded as D5.2 (45h).  • When operating at 8.0 GT/s or above: TS2 Identifier. Encoded as 45h. |
| 14 - 15 | • When operating at 2.5 or 5.0 GT/s: TS2 Identifier. Encoded as D5.2 (45h).  • When operating at 8.0 GT/s or above: TS2 Identifier (encoded as 45h) or a DC Balance Symbol. |

#### 6.4.1.3. Modified TS1/TS2 (8b/10b encoding)

|  |  |
| --- | --- |
| Symbol Number | Description |
| 0 | COM (K28.5) for Symbol alignment. |
| 1 | Link Number.  Downstream Ports: 0-31, PAD (K23.7).  Upstream Ports: 0-255, PAD (K23.7). |
| 2 | Lane Number within Link : 0-31, PAD. PAD is encoded as K23.7. |
| 3 | N\_FTS. The number of Fast Training Sequences required by the Receiver: 0-255. |
| 4 | Data Rate Identifier  BIT 0 - Reserved for future Data Rate.  BIT 1 - 2.5 GT/s Data Rate Supported. Must be set to 1b.  BIT 2 - 5.0 GT/s Data Rate Supported. Must be set to 1b if Bit 3 is 1b.  BIT 3 - 8.0 GT/s Data Rate Supported. Must be set to 1b if Bit 4 is 1b.  BIT 4 - 16.0 GT/s Data Rate Supported. Must be set to 1b if Bit 5 is 1b.  BIT 5 - 32.0 GT/s Data Rate Supported.  ***BIT 6 -*** *Link Upconfigure Capability.*  BIT 7 - Reserved. |
| 5 | Training/ Equalization Control  BIT 0 - Equalization bypass to highest rate support. See Section 4.2.3  BIT 1 - No Equalization needed. See Section 4.2.3  BIT 3:2 - Reserved  BIT 4 - Retimer Present bit  0b - No Retimers present  1b - One Retimer is present  BIT 5 - Two or more Retimers Present  BIT 6 - 1b  BIT 7 - 1b |
| 6 | For Modified TS1: TS1 Identifier, encoded as D10.2  For Modified TS2: TS2 Identifier, encoded as D5.2 |
| 7 | For Modified TS1: TS1 Identifier, encoded as D10.2  For Modified TS2: TS2 Identifier, encoded as D5.2 |
| 8 - 9 | ***BIT 2:0 - Modified TS Usage***  000b - PCIe protocol only  001b - PCIe protocol only with vendor defined ***Training Set Messages***  ***010b - Alternate Protocol Negotiation***  Reserved  011b through 111b - The values advertised in these bits must be consistent with the Modified TS Usage Mode  Selected field of the 32.0 GT/s Control register and the capabilities of the device. These are  bits[2:0] of Symbol 8.  ***BIT 15:3 - Modified TS Information 1***  If Modified TS Usage = 001b or 010b; else Reserved. |
| 10 - 11 | ***Training Set Message Vendor ID*** if Modified TS Usage = 001b.  ***Alternate Protocol Vendor ID*** if Modified TS Usage = 010b.  Reserved for other cases. |
| 12 - 14 | If Modified TS Usage = 001b or 010b, ***Modified TS Information 2***  Else, Reserved |
| 15 | Bit-wise even parity of Symbols 4 through 14. . For example: Bit 0 = Symbol 4 Bit [0] ^ Symbol 5 Bit [0] ^ …. ^ Symbol 14  Bit [0], … , Bit [7] = Symbol 4 Bit [7] ^ Symbol 5 Bit [7] ^ …. ^ Symbol 14 Bit [7] |

### **6.4.2. Electrical Idle Sequences (EIOSQ)**

Before a Transmitter enters Electrical Idle, it must always send an Electrical Idle Ordered Set Sequence (EIOSQ), unless otherwise specified. An Electrical Idle Ordered Set Sequence (EIOSQ) is defined as one EIOS if the current Data Rate is 2.5 GT/s, 8.0 GT/s, 16.0 GT/s, or 32.0 GT/s Data Rate, or two consecutive EIOSs if the current Data Rate is 5.0 GT/s.

#### 6.4.2.1. EIOS (Electrical Idle Ordered Set)

Gen 1 & 2

|  |  |
| --- | --- |
| Symbol Number | Description |
| 0 | COM (K28.5) for Symbol alignment |
| 1 | IDL (K28.3) |
| 2 | IDL (K28.3) |
| 3 | IDL (K28.3) |

Gen 3 and above

|  |  |
| --- | --- |
| Symbol Number | Description |
| 0 - 15 | EIOS (66h) Identifier and Payload |

#### 6.4.2.3. EIEOS (Electrical Idle Exit)

Gen 2

|  |  |
| --- | --- |
| Symbol Number | Description |
| 0 | COM (K28.5) for Symbol alignment |
| 1 - 14 | EIE (K28.7) - K Symbol with low frequency components for helping achieve exit from Electrical Idle |
| 15 | TS1 Identifier (not scrambled) |

Gen 3

|  |  |
| --- | --- |
| Symbol Number | Description |
| 0, 2, 4, 6, 8, 10, 12, 14 | Symbol 0: EIEOS Identifier  A low frequency pattern that alternates between eight 0s and eight 1s. (value 00h). |
| 1, 3, 5, 7, 9, 11, 13, 15 | A low frequency pattern that alternates between eight 0s and eight 1s. (value FFh). |

### **6.4.3. Fast Training Sequence (FTS)**

Fast Training Sequence is the mechanism that is used for bit and Symbol lock when transitioning from L0s to L0. The FTS is used by the Receiver to detect the exit from Electrical Idle and align the Receiver’s bit and Symbol receive circuitry to the incoming data.

Gen 1

|  |  |
| --- | --- |
| Symbol Number | Description |
| 0 | COM (K28.5) for Symbol alignment |
| 1 | FTS (K28.1) |
| 2 | FTS (K28.1) |
| 3 | FTS (K28.1) |

### **6.4.4. SKIP (SKP)**

SKP Ordered Sets are used to compensate for differences in frequencies between bit rates at two ends of a Link. The Receiver Physical Layer logical sub-block must include elastic buffering which performs this compensation. The interval between SKP Ordered Set transmissions is derived from the Transmit, Receiver, and Refclk specifications

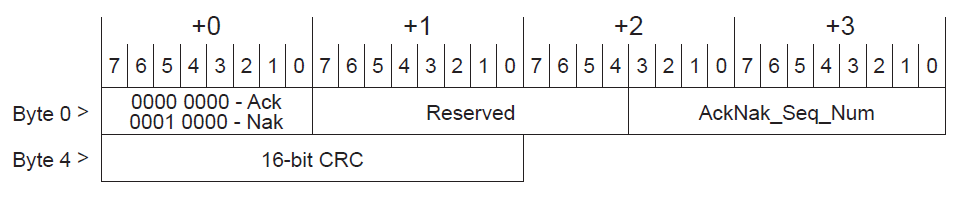
Gen 1

|  |  |
| --- | --- |
| Symbol Number | Description |
| 0 | COM (K28.5) for Symbol alignment |
| 1 | SKP (K28.0) |
| 2 | SKP (K28.0) |
| 3 | SKP (K28.0) |

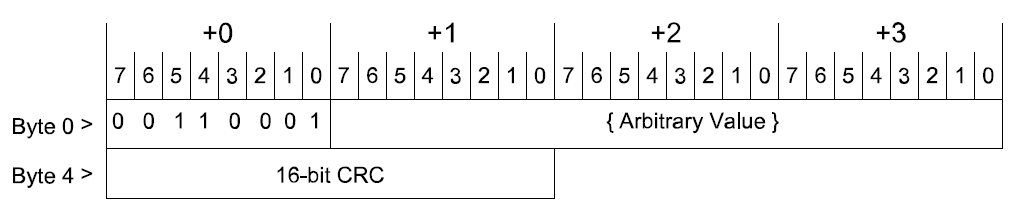
\*Changes may occur according to different situations.

## **6.5. Data Link Layer Packets (DLLPs)**

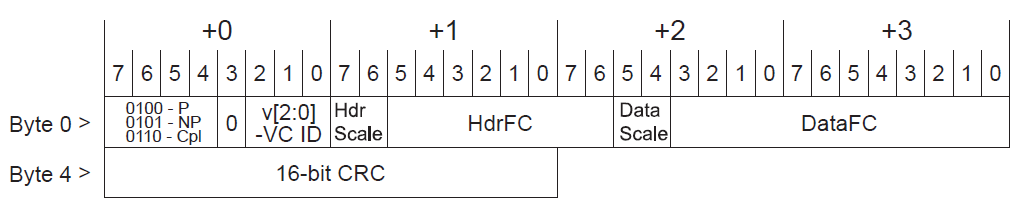
### **6.5.1. Ack / Nak**



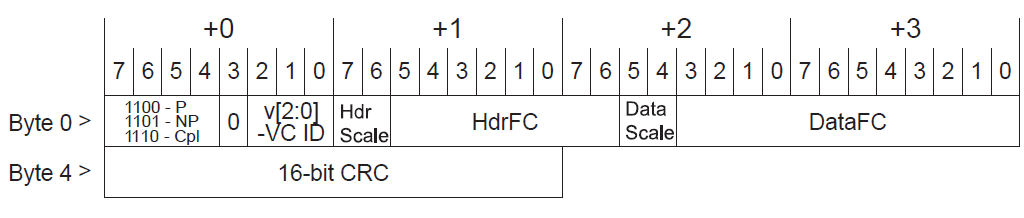
### **6.5.2. NOP**



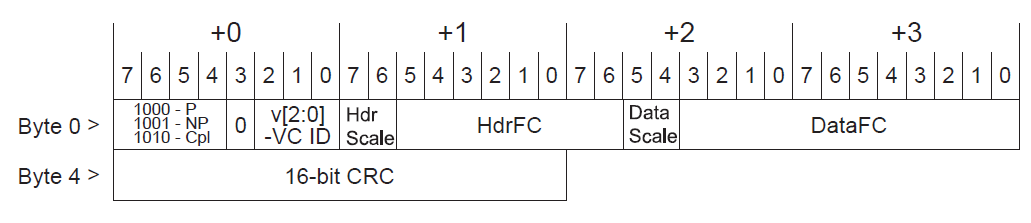
### **6.5.3. InitFC1**



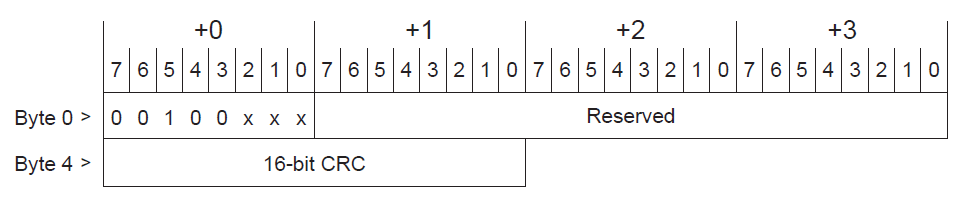
### **6.5.4. InitFC2**



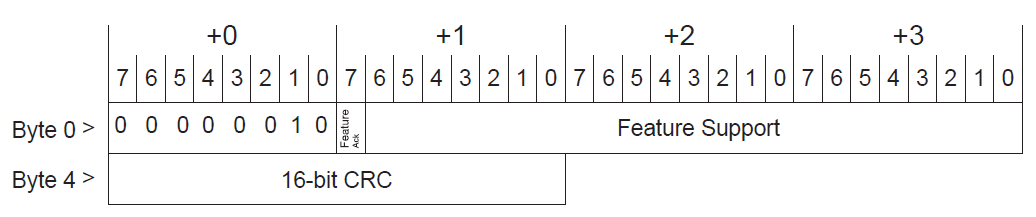
### **6.5.5. UpdateFC**



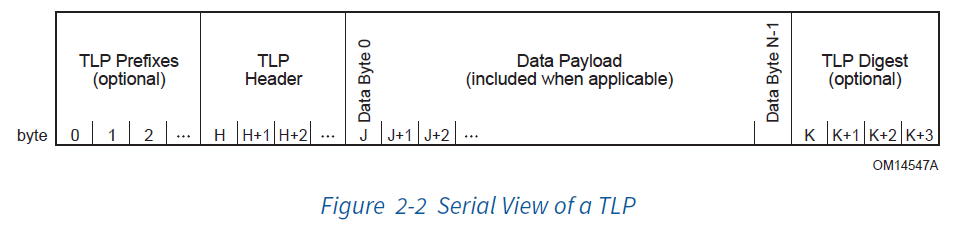
### **6.5.6. PM**



### **6.5.7. Feature**

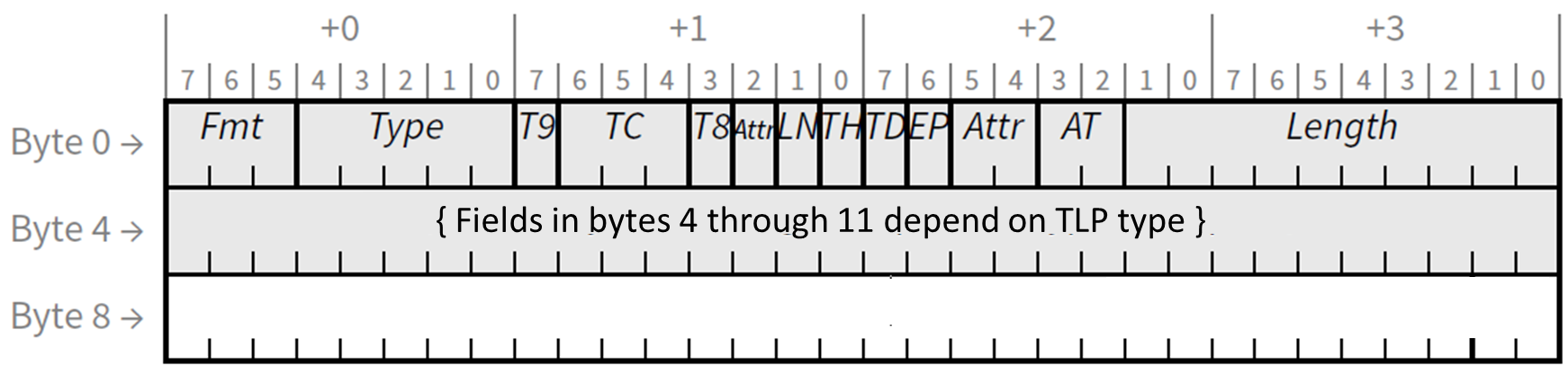


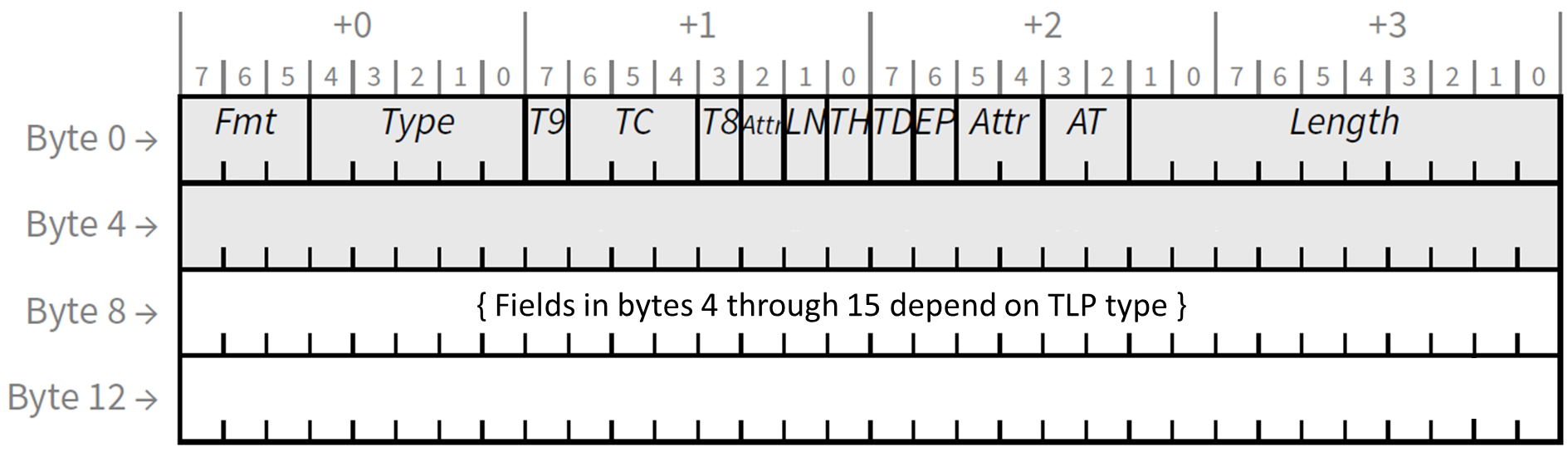
## **6.6. Transaction Layer Packets (TLPs)**



### **6.6.1. General TLP Header**

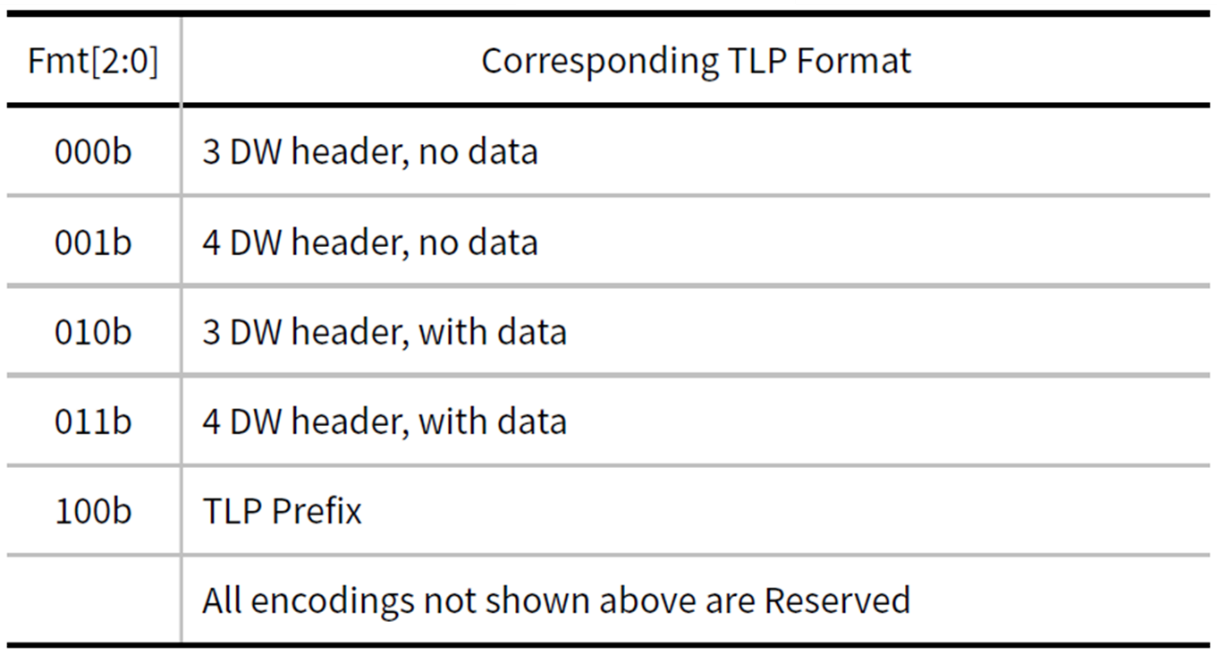
#### 6.6.1.1. Layout

****1. 3 DW (DW = 32bit) Packet:

2. 4 DW (DW = 32bit) Packet:****

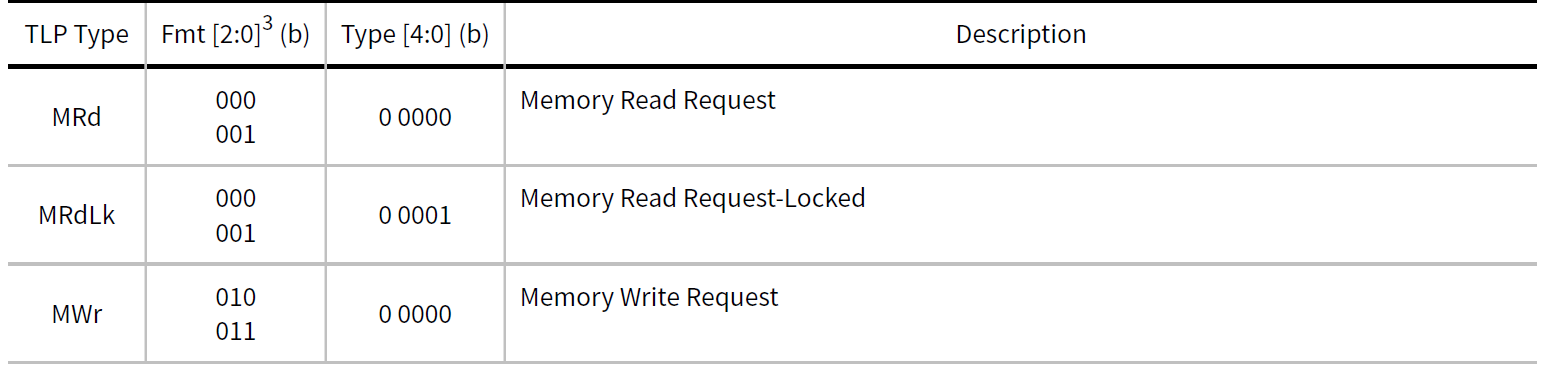
#### 5.6.1.2. Fmt Field

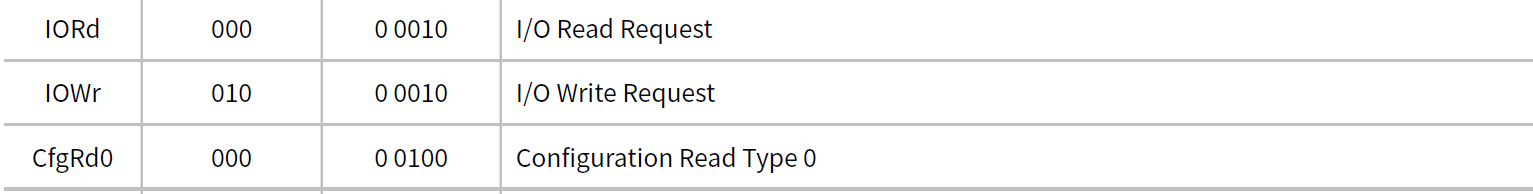
Determines TLP format. bits 7:5 of byte 0

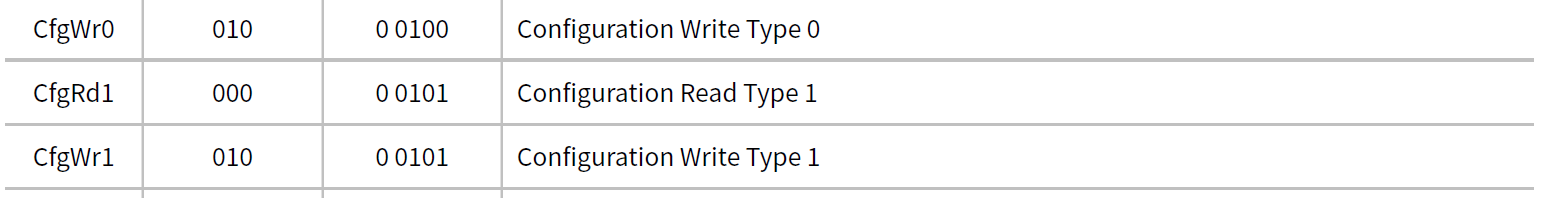
****

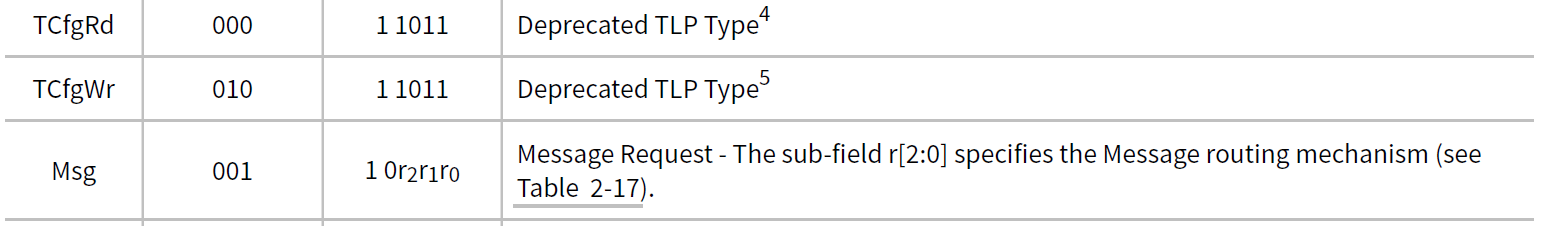
#### 5.6.1.3. Type Field

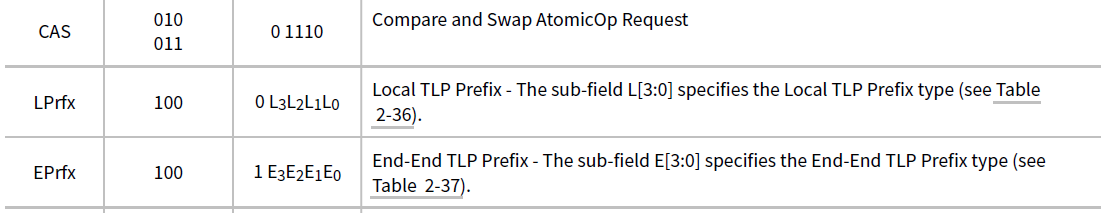
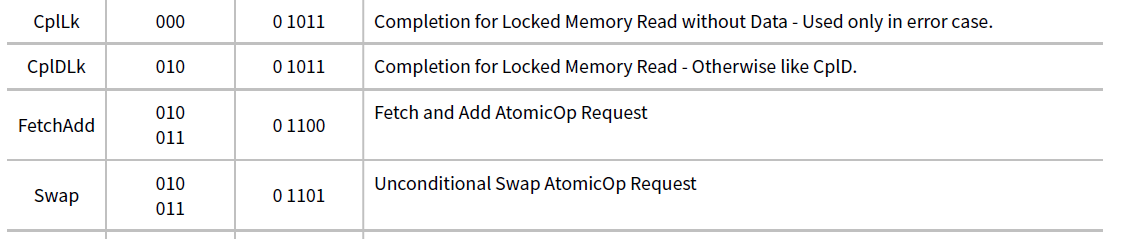
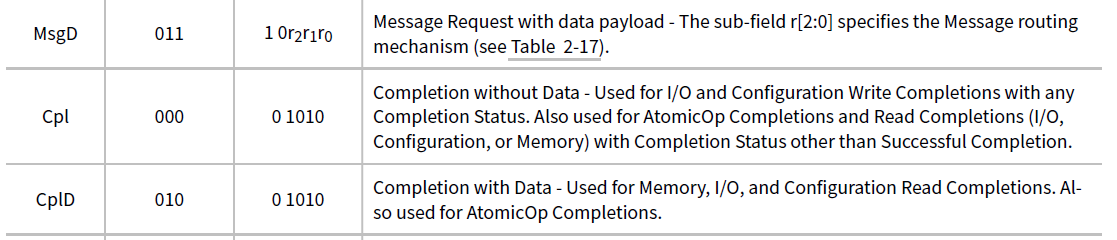
Determines TLP type. bits 4:0 of byte 0



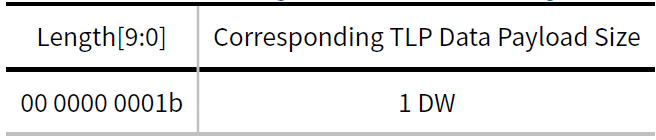


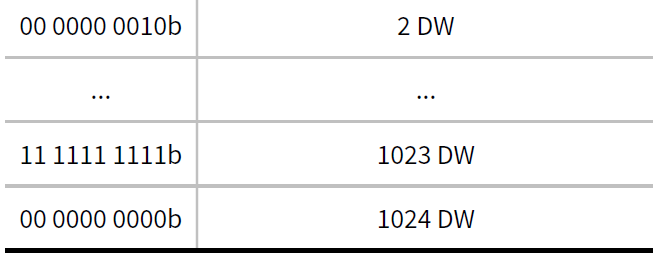


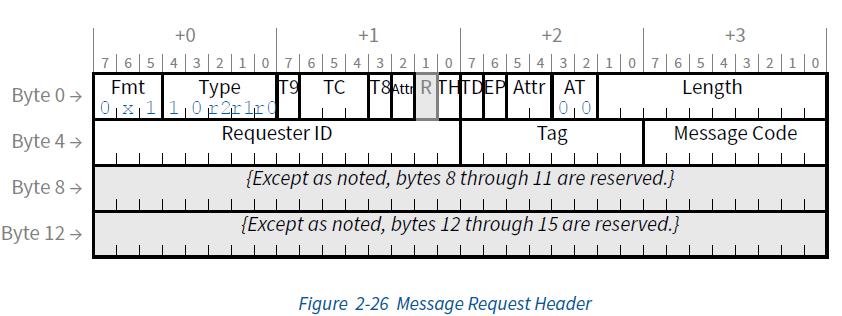




#### 5.6.1.3. Length Field

Data payload length in DW (DW = 32bit)



**for more information refer to 2.2.8 Message Request Rules page 137**

**NCB-PCI Express Base 5**

# **7. Referenced Documents**

1. PCI Express® Base Specification Revision 5.0 Version 1.0 PCI-SIG 14 March 2019

2. 8b/10b Encoder/Decoder, Reference Design RD1012, January 2015,

LATTICE SEMICONDUCTORE.

3. PCI Express System Architecture, MINDSHARE

**3.6.2 LCRC, Sequence Number, and Retry Management (TLP Transmitter)**

The TLP transmission path through the Data Link Layer (paths labeled 1 and 3 in Figure 3-1) prepares each TLP for transmission

by applying a sequence number, then calculating and appending a Link CRC (LCRC), which is used to ensure the

integrity of TLPs during transmission across a Link from one component to another. TLPs are stored in a retry buffer, and

are re-sent unless a positive acknowledgement of receipt is received from the other component. If repeated attempts to

transmit a TLP are unsuccessful, the Transmitter will determine that the Link is not operating correctly, and will instruct

the Physical Layer to retrain the Link (via the LTSSM Recovery state, Section 4.2.6). If Link retraining fails, the Physical

Layer will indicate that the Link is no longer up, causing the DLCMSM to move to the DL\_Inactive state.

The mechanisms used to determine the TLP LCRC and the Sequence Number and to support Data Link Layer Retry are

described in terms of conceptual “counters” and “flags”. This description does not imply nor require a particular implementation

and is used only to clarify the requirements

***DL\_Inactive***

◦ Initial state following PCI Express hot, warm, or cold reset (see Section 6.6). Note that DL states are

unaffected by an FLR (see Section 6.6).

◦ Upon entry to DL\_Inactive

▪ Reset all Data Link Layer state information to default values

▪ If the Port supports the optional Data Link Feature Exchange, the Remote Data Link Feature

Supported, and Remote Data Link Feature Supported Valid fields must be cleared.

▪ Discard the contents of the Data Link Layer Retry Buffer (see Section 3.6)

***4.2.4.1 Training Sequences***

Training sequences are composed of Ordered Sets used for initializing bit alignment, Symbol alignment and to exchange

Physical Layer parameters. When the data rate is 2.5 GT/s or 5.0 GT/s, Ordered Sets are never scrambled but are always

8b/10b encoded. When the data rate is 8.0 GT/s or higher, the 128b/130b encoding is used and Symbols may or may not

be scrambled, according to the rules in Section 4.2.2.4.